

Application No.: 10/072,339

Docket No.: TKHR5060-D

REMARKS**Present Status of the Application**

The Office Action mailed March 20, 2003, rejected all presently-pending claims 8-14. Specifically, the Office Action rejected claims 8-14 under 35 U.S.C. 103(a), as being anticipated by Gardner et al. (U.S. 6,096,591 → '591) in view of Divakaruni et al (U.S. 6,429,068 → '068). Claims 8-14 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Claim Rejections-35 USC 103

The Office Action rejected claims 8-14 under 35 U.S.C. 103(a), as being anticipated by Gardner et al. (U.S. 6,096,591 → '591) in view of Divakaruni et al (U.S. 6,429,068 → '068).

Applicants respectfully traverse the rejections for at least the reasons set forth below. The present invention is directed to a high-resistive thin film resistor. The claim 8 reads:

Claim 8 (Currently Amended) A high resistive thin film resistor structure comprising:
a substrate having an isolation region and an active region;
a patterned, lightly doped polysilicon layer located on and in contact with the isolation region;
a diffusion barrier layer located above the lightly doped polysilicon layer; and
a spacer located on the sidewalls of the lightly doped polysilicon layer and the barrier diffusion layer.

According to the Examiner, the cited '591 patent discloses a high resistive thin film resistor structure comprising a substrate (202) having a isolation region (276) and an active region (208), a patterned lightly doped polysilicon layer (124) located above the isolation region,

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but not in contact with the isolation region, a diffusion barrier layer (122) and a spacer (142) located on the sidewalls of the lightly doped polysilicon layer and the barrier diffusion layer. Further, the Examiner asserts that the cited patent '591 teach the barrier layer (250) located above the polysilicon layer (221) and the polysilicon layer (221) in contact with the isolation region (208).

Applicant respectfully disagrees with the Examiner's interpretation of '591. Refer to col. 5, lines 53-63 of '591, the polysilicon layer 124 is etched to form a polysilicon gate 128, as shown in FIG. 1H. The doped concentration of the polysilicon gate is heavy, while that of the thin film resistor is light, so that the electric characteristic curve of the polysilicon gate and that of the thin film resistor are different. Therefore, the function of the polysilicon gate and that of the thin film resistor are entirely different. For example, the thin film resistor is used for limiting or reducing current, while the polysilicon gate of '591 is used as a switch. Hence, it is no way that '591 polysilicon gate are comparable to the thin film resistor of the present invention.

Furthermore, refere to col. 4/8, line 33-34/17-18 of '591, the substrate 102/202 of have two regions including a resistor region 106/206 and an active region 108/208. The resistor region 106/206 is used for forming a diffused resistor 120/220 (Col. 5/8, line 13/64-65), and the active region 108/208 is used for forming insulated-gate field-effect transistor (IGFET) (Col. 8/9, line 64-65/3). The structure formed on the active region 108/208 of the cited '591 patent has restricted to IGFET, and the structure formed on the resistor region has restricted to the diffused

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resistor. Therefore, there is no motivation and no purpose to modify the polysilicon gate of IGFET as a resistor, since the resistor disclosed was on the resistor region 106/206.

Further, the polysilicon layer of '591 is formed on the gate oxide layer 122, rather than formed on and in contact with the isolation region as required by claim 8. Clearly, the '591 patent fails to teach or suggest "*a patterned, lightly doped polysilicon layer located on and in contact with the isolation region*". Clearly, gate 128 cannot be modified to be located on and in contact with the isolation region, because that would destroy its structural identity and would be against its intended purpose.

As acknowledged in the Office Action, the '591 patent fails to teach or suggest "*a diffusion barrier layer located above the lightly doped polysilicon layer*".

Further, the high resistive thin film resistor structure of the present invention as define in claim 8 comprises "a spacer located on the sidewalls of the lightl doped polysilicon layer and the barrier diffusion layer". The '591 patent does not teach or suggest such a spacer structure. The Office Action has identified doped polysilicon layer 124 and diffusion barrier layer 122 of the '591 patent as equivalent to that recited in claim 8. However, the spacer (142) in the '591 patent is located only on the sidewall of the gate 128 and does not cover the sidewall of the layer 122.

The Office Action noticed that Gardner lacks the diffusion layer located above the polisicon layer, but cited '068 patent teaches a barrier layer 250 located above the polysilicon layer (221). Applicant respectfully submits that the proposed combination is improper for the reason set forth below.

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The polysilicon layer 221 in FIG. 2 of '068 extends on the isolation 208 and is covered by a barrier layer 250, but the structure shown in FIG. 2 is a process structure, rather than a final structure. The barrier layer 250 and the polysilicon layer 221 extending on the isolation 208 are removed after the gate stacks in the support region 206 are patterned as shown in FIGS. 3 and 4, refer to col. 8, lines 63-64. That is, the barrier layer 250 and the polysilicon layer 221 extending on the isolation 208 of FIG. 2 did not need in the final structure of FIG. 10. In other words, there is no motivation and no purpose to modify the gate structure of polysilicon gate 128 and gate oxide layer 122 in '591 with the layers to be removed of '068. Thus, the proposed combination is improper and cannot support the rejection under 35 U.S.C. 103.

Further, the '068 patent clearly cannot cure the above discussed deficiencies of '591. Therefore, even if '591 and '068 were combined as proposed, the combination would still fail to disclose all the features of claim 8.

For at least the reason discussed above, Applicant respectfully submits that the amended independent claim 8 patentably defines over *Gardner et al* and *Divakaruni et al*. For at least the same reason, dependent claims 9-14 also define over *Gardner et al* and *Divakaruni et al* since they are dependent on claim 8.

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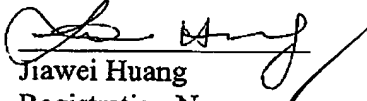
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CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 8-14 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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